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(FPGA) of a turbo decoder for 3GPP long-term evolution (LTE) standard, respectively, for IEEE 802.16-based WiMAX systems. We initially present the serial decoding architectures for the two systems.

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Implementation of physical downlink control channel (PDCCH) FOR LTE using FPGA Abstract: LTE is accepted worldwide as the Long Term Evolution Perspective for today's 3G and 4G networks. The downlink physical channels of LTE include 3 data channels (PDSCH, PMCH and PBCH) and 3 control channels (PDCCH, PCFICH and PHICH).

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Implementing LTE on FPGAs. Here's a review of the LTE algorithms and a practical implementation on a Xilinx FPGA. The reference design is tested using multiple video stream with varying encoding rates. By Rob Payne, Xilinx. dspdesignline.com (February 06, 2009) The next generation of the 3GPP wireless standard is called long-term evolution (LTE). It provides a leap in performance and a complete move to packet-based processing.

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Efficient FPGA Implementation of a CTC Turbo Decoder for ...

Implementation of an efficient turbo decoder with low complexity, short delay and insignificant performance degradation is currently a quite challenging task. The paper presents an implementation of a 3GPP TS 36.212 LTE turbo decoder. The design of the turbo decoder has been optimized to achieve efficient FPGA resource utilization.

FPGA implementation of LTE turbo decoder using MAX-log MAP ...

FPGA Implementation of UFMC Based Baseband Transmitter: Case Study for LTE 10MHz Channelization Atif Raza Jafri , 1 Javaria Majid , 1 Lei Zhang , 2 Muhammad Ali Imran , 2 and M. Najam-ul-Islam 1 1 Electrical Engineering Department, Bahria University, Islamabad, Pakistan

FPGA Implementation of UFMC Based Baseband Transmitter ...

Abstract- In the long- term evolution(LTE) physical layer, using turbo code is considered the core of the error-correcting code. This paper presents an implementation of LTE turbo decoding using the Log- Maximum a posteriori (MAP) algorithm with reduced number of required cycles approximately by 75% based on serial to parallel operation.

DIFFERENT FPGA PRODUCTS BASED IMPLEMENTATION OF LTE TURBO CODE

FPGA Implementation of Turbo Decoder for LTE Standard Abstract- In the long- term evolution(LTE) physical layer, using turbo code is considered the core of the error-correcting code.

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Abstract. This paper presents a FPGA implementation of an OFDMA modem for the physical layer of LTE technology, suitable for both uplink and downlink transmission. The designed structure achieves a low area occupation while fulfilling LTE requirements. 9.3-3 , , ,Design and FPGA implementation of an OFDMA ,baseband modem for 3GPP-LTE physical layer ,F. J. López,,Martínez , E. del Castillo,,Sánchez, E. Martos,,Naya, J. T. Entrambasaguas , ,Communication Engineering Department, University ...

Design and FPGA implementation of an OFDMA baseband modem ...

Using fewer than 18 bits for the coefficients minimizes the number of DSP blocks required for an FPGA implementation. The input to the DDC filter chain is 16-bit data with 15 fractional bits. The filter outputs are 18-bit values, which provides extra headroom and precision in the intermediate signals.